**Decoders**

**OBJECTIVE:**

![Shape

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![Shape

Description automatically generated with medium confidence](data:image/png;base64,iVBORw0KGgoAAAANSUhEUgAAAFwAAAB7CAYAAAD5RufWAAAABmJLR0QA/wD/AP+gvaeTAAAACXBIWXMAAA7EAAAOxAGVKw4bAAAA6UlEQVR4nO3bSw6CUBAEQPT+d9bVbEyUj48GhqoDyJtOQ4KO0wQAAAAAAAAAAAAAAAAAAAAAAADAdo/Bn/cKX+9yRgQwF/Ke176cf4beGvTIM1zOlmFHBf3pFsGvHXKvsEv70NcMuHfYpXXoS4dLhV3ahr5ksHTYpWXoz6MPcDdzLTqq3aVdyzU87FeDjm53adVyDQ8TeNi32/Usj5PS5rGi4WECDxN4mMDDBB4m8DCBh3m1D9PwMIGH+T48TMPD/KYZpuFh1iTCLAKFWXULs8wZZl05zEJ+mL+cAAAAAAAAAAAAAAAA5/cGjgkVNMKrI4MAAAAASUVORK5CYII=)To learn the concept of enabling a signal (active-low and active-highenable)

**APPARATUS:**Logic trainer, Logic probe

**COMPONENTS:**ICs 74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS139.

**THEORY**

**Enabling:**

The concept of enabling is to permit an input signal to pass through or is blocked completely. The enable bit is also used to enable or disable the normal functioning of a logic circuit. A logic circuit can be enabled or disabled using a single enable bit. This enable bit can be either active low or active high. Let us have an example of an AND gate with enable bit. If the enable bit is active high then it means that the AND gate performs normal operation if the enable bit is one else the output of AND gate is forced to bezero.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | | **Output** |
| **E** | **A** | **B** |  |
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Circuit Diagram:**

Diagram

Description automatically generated

If the enable bit is active low then it means that the AND gate performs normal operation if the enable bit is zero else the output of AND gate is forced to be zero.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | | **Output** |
| **E** | **A** | **B** |  |
| 1 | X | X | 0 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |

**Circuit Diagram:**

A picture containing diagram

Description automatically generated

**Decoder:**

A decoder is a combinational circuit that decodes the encoded inputs. A binary decoder has ***n*** inputs and a maximum of ***2n***outputs. An n-bit binary number provides ***2n***minterms or maxterms. The decoder indicates one of the ***2n***minterms or maxterms at the outputs based on the input combinations. The decoder that produces ***2n***minterms as its outputs is said to be a decoder with active high outputs, whereas, the decoder that produces ***2n***maxterms as its outputs is said to be a decoder with active low outputs. Let us take ***n***=2 as an example, so that we obtain the 2-to-4 line decoder with active high outputs. Figure 7-1 shows the block diagram of 2x4 decoder.

Text

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**Figure 7-1 2x4 decoder**

**Truth Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | **Outputs** | | | |
| **A** | **B** | **D0** | **D1** | **D2** | **D3** |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

**Boolean Expressions of Outputs:**

**D0: D1: D2: D3:**

The Boolean expressions show that four outputs of 2x4 decoder show four minterms of two binary variables **A** and **B**.

**Circuit diagram for 2x4 decoder with active high outputs:**

Diagram, schematic

Description automatically generated

**2-to-4 line decoders:**

Now, we will use **74LS139** as deocder. 74LS139 IC contains two fully independent **2-to-4 line decoders with active low enables.** The function table and connection diagram for this IC are shownbelow:

**Function Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Enable** | **Inputs** | | **Outputs** | | | |
| **G** | **B** | **A** | **Y0** | **Y1** | **Y2** | **Y3** |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H= Logic High, L= Logic Low, X= Don‟t Care

**Connection Diagram:**

Diagram

Description automatically generated

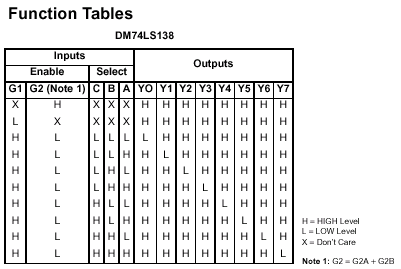
**LAB TASK # 1:**

Design and implement a 2-to-4-line decoder **combinational circuit diagram** with enable input (E) on **Logic Trainer only**. When E is High, the decoder will operate normally, when E is Low, all outputs should be off regardless of the inputs.

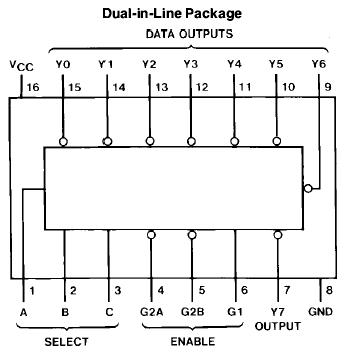
1. Make the truth table
2. Write equations of min and max terms of this decoder (part a).
3. In the space given below, draw 2x4 decoder along with the logicdiagram.

**3-to-8 line decoders:**

74LS138 IC contains 3-to-8 line decoder. The function table and connection diagram for this IC are shown below:

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**Connection Diagram:**



**LAB TASK # 2:**

1. Three PCs are sharing a single printer. Design a logic circuit that displays how many PCs are sending print request to the printer at a time. The count is displayed on LEDs. Also make the truth table and implement this circuit on **Logic Works only.**
2. Design a 3-to-8-line decoder using two 2-to-4 line decoders and a NOT gate. Carefully observe this that the IC provided to you is with **active low outputs and active low enables**. Implement this circuit on **Logic Works only.**